Acceptance Testing of the JTIDS Class II Terminal by Augmented Minicomputer

Monte H. Wallenstein*
The Singer Company, Wayne, N.J.

A Class II terminal for the Joint Tactical Information Distribution System (JTIDS) is being developed by The Singer Company, Kearfott Division. The unique features of JTIDS are the communication connectivity provided between participants, the high-capacity secure digital communications, and the relative navigation capabilities. The digital communication among members is achieved by utilizing a time division multiple access (TDMA) data link. As part of the terminal development, the system must undergo extensive testing. This paper describes the minicomputer based test facility that was built to test the entire terminal complex consisting of a digital microprocessor, a receiver-transmitter, a TDMA signal processor, and TACAN signal processor, by simulating both a real-world JTIDS TDMA community and all peripheral integrated avionics. The facility's ability to control, test, and verify results while providing for operator flexibility is also described. The paper emphasizes the methods used for system testing, particularly the coordination of the high data rates involved in a time-constrained TDMA system.

Introduction

THE Singer JTIDS Class II terminal provides time division multiple access (TDMA) communication and navigation capabilities for aircraft, ships, and mobile ground facilities. The terminal is undergoing an extensive series of tests prior to customer delivery. These tests include hardware testing, software validation testing, acceptance testing, and system demonstration. The contents of this paper describe the verification testing of the highly complex time division multiple access system. Prior to describing the methods used in testing the TDMA system, a description of what JTIDS is and how a TDMA system works is presented.

Background

The Joint Tactical Information Distribution System (JTIDS) is a joint service development program. Its purpose is to provide high-capacity secure digital communication, relative navigation, and user identification. The unique feature of JTIDS is the connectivity provided among its participants interms of communications and relative navigation. It can be thought of as providing a dynamically updated information base which can be addressed by any user for purposes of drawing out or adding data. The JTIDS program plan calls for the development of three classes of equipment. Class I terminals will be used on large aircraft and some ships in a variety of command and control applications. Class II terminals will be installed on user platforms where space and weight are generally at a premium. The Singer-Kearfott Class II platform designated as the AN/URQ-28 is applicable to tactical aircraft, smaller ships, and mobile ground units. Class III terminals will be based on low'cost design techniques and will be used for missile guidance, manpacks, etc.

Present command and control systems are limited by their communication capability. Current data links provide limited data rate capability, poor antijamming characteristics, and exploitable qualities in a constrained architectural configuration. Current systems also lack navigation consistency among their units. These systems have provided inadequate time correlation of multiple-platform sensor data and insufficient identification of friendly forces. The JTIDS system provides a high communication rate capacity, utilizing a time division multiple access data link, which can support fixed-format message exchanges, free test messages (such as secure digital voice), and multiple net operation. By defining a common relative grid of operation, each member can navigate using the common relative navigation grid. In addition, identification of cooperative grid members is an inherent feature of the JTIDS-equipped community members.

The JTIDS time division multiple access system is a highly advanced information distribution system. The TDMA system offers high data capacity to multiple subscribers in a short period of time. The means of transmitting and receiving are highly resistant to the electronic countermeasures of modern day jammers, and are cryptographically secure against eavesdropping or exploitation. The TDMA concept increases system communication reliability, decreases vulnerability to eavesdropping and atmospheric conditions, and conserves the overcrowded frequency spectrum. The combination of the capabilities of the digital computer, with its ability to precisely control functions in a time-ordered sequence, and the unique use of the time spectrum permits the JTIDS TDMA system to provide advances which were not available in recent years.

The capability of JTIDS is shared among participants on the basis of time division, using the technique known as time division multiple access (TDMA). Each participant in the JTIDS network is assigned a sufficient number of time slots to accommodate the number of messages likely to be transmitted by him for his mission. During his assigned transmit time slots, each user broadcasts data into a commonly accessible communications data stream represented by a TDMA ring. All other elements can extract information of the type they require by continuously monitoring and sampling the data base. Digital processing provides each participant with secure access to all of the information generated by the other elements by applying fixed and variable filters to the incoming messages. Participants who have information will broadcast that information routinely into the net without needing to know who the recipients may be, and tactical elements needing the data will extract it from the net without needing to know who furnished it. The user does not need to request

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*Engineering Specialist, Kearfott Division.

information from a specific party, or to wait until he is notified by information important to his mission. Instead, he decides what category of data he wants and then receives everything the system has in that category from the data base stored in the computer. An individual message inserted into the data base may be intended for general dissemination or it may be addressed to one or more discrete recipients. Consequently, JTIDS simultaneously effects communication from one element to many elements, from one to one, from many to one, or from many to many. Figure 1 illustrates the JTIDS TDMA slot structure. The TDMA slots are organized in epochs of 12.8 minutes. Each epoch consists of 64 cycles containing 1536 slots. Each slot is 7.8125 milliseconds consisting of guard time, sync, and message. The JTIDS TDMA system also has the capability of offering transmissions from many elements on multiple nets in a single slot in order to provide optimum use of the spectrum by employing code division and frequency division. Code and frequencies are computer controlled and thus the net selection can be automatic or controlled by the user. Thus, JTIDS allows for multiple communities, each community being made up of multiple users all operating in a carefully choreographed ballet of time and frequency assignment.

A single JTIDS net is capable of transmitting or receiving 60 kilobits of information per second. Since current digital voice transmission requires 16K bits per second, over 40 K bits per second are available for other types of data transfer. The system transmits bursts of information which are synchronized and sequenced in time. The terminal's microprocessor must perform hundreds of thousands of operations per second. It must recognize when it is to transmit, accepting various types of messages from the terminal's I/O ports, sorting, and holding these messages until the assigned transmit slot is available. The microprocessor must also perform its own relative navigation computations. This is accomplished by receipt of certain specific messages transmitted by other members, and by using them with time-of-arrival measurements as observables in a Kalman filter, which estimates errors in its own dead-reckoning sensor devices attached to the terminal. The terminal microprocessor must also inform others of its own position by generating position reports in fixed-format messages. In addition, the terminal has the ability to process the TACAN waveform to determine bearing and range to a TACAN beacon station.

System Definition and Test Setup

The acceptance testing of a JTIDS terminal requires testing under simulated real-world condition in order to verify that all hardware-to-hardware and hardware-to-software interrelated functions are operating. The acceptance tests must demonstrate that the JTIDS terminal is capable of transmitting specific messages in assigned time slots (7.8125 ms) and receiving messages in other specified slots (a slot being defined as the basic time unit common to all members for transmitting or receiving messages). Also to be demonstrated is the terminal's ability to accept and deliver to another computer – specified as the Fixed Format Message Processor – messages that have preassigned formats. The terminal must also be capable of interfacing with a Free Text Message Processor. Free text messages have no specified format except as specified by the Free Text Message Processors themselves, and can only be transmitted or received by the terminal upon special request by the Free Text Message Processor. The terminal must also be capable of performing the relative navigation computations, and uses a Kalman filter to estimate dead-reckoning equipment navigation errors. The terminal must be capable of accepting sensor data and supplying sensor corrections upon demand. The terminal, when in a TACAN processing mode, must be capable of driving a TACAN display. All terminal functional operations are controlled from a mode control unit (MCU) which is system-operator controlled. The acceptance testing facility was designed to test all these functions, from message receipt from a processor to transmission, or receipt from another terminal via the RF link to transfer of the decoded and processed message to the appropriate processor via the appropriate I/O ports.

Figure 2 illustrates two-terminal communication and shows the associated terminal processor. A requirement of the test setup is that all of the interfaces within the dotted lines be tested. These interfaces and their associated processors could be simulated by a single minicomputer.

The test complex using this minicomputer is illustrated in Fig. 3. It consists of a general purpose minicomputer which, as will be described later, is used to control, test, and verify results. The minicomputer is connected via two DMA channel lines, and steering and control logic, to two terminals: the test terminal and the terminal being tested. The test terminal is required to drive the RF port of the terminal being tested. Each terminal generates its own time interrupt which is being used to coordinate the transfer and receipt of data to the minicomputer. The time interrupt, issued every 7.8125 ms, is the basic computation cycle of each terminal. The test complex minicomputer is then responsible to handle the two asynchronous time interrupts. The minicomputer could, in every slot, transfer and receive data from each terminal as illustrated in Fig. 4. The minicomputer is attached to five I/O peripheral equipments: magnetic tapes for driving functions and data recording, a disk for program storage, a line printer for hard copy of test steps and printout of results utilized in system verification, and a keyboard/CRT device for operator test control and data entry.

The steering and control logic (SCL), one for each terminal interface, controls the computer-to-terminal data transfer and port activation controller. In transmitting data to a specific port of a terminal, the minicomputer informs the SCL by setting a bit in the validity word (word 1) as to which segment of the data block (Fig. 4) is to be transferred. The SCL strips the data and activates the required terminal port for receipt of the data. In receiving data by the minicomputer, the SCL accepts data from the terminal port and loads the associated area of the data buffer prior to transmitting the buffer to the minicomputer, with an indication in the validity word as to which segment is valid.

The test terminal (TT) will utilize a core memory for software modifications throughout the acceptance testing schedule. The terminal or unit that is under test (UUT) will contain a solid-state memory. Each terminal is connected to its own MCU, which is test-operator controlled.

Two simulators will be coupled to the RF link. The first simulator will simulate a TACAN beacon in order to test the TACAN processing capability of the terminal or unit under test. The jamming signal will simulate radio interference that may be present in the environment.

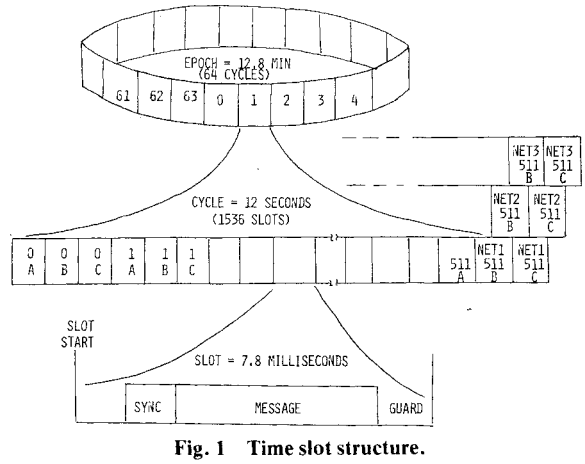

Fig. 1 Time slot structure.

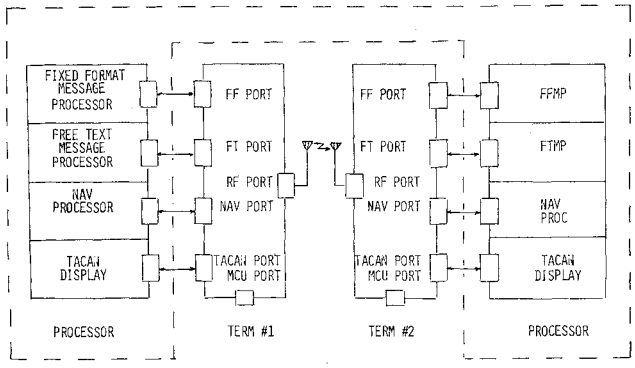

Fig. 2 Terminal operation.

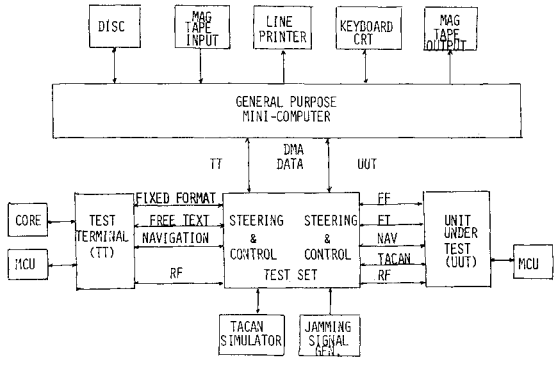

Fig. 3 Test complex.

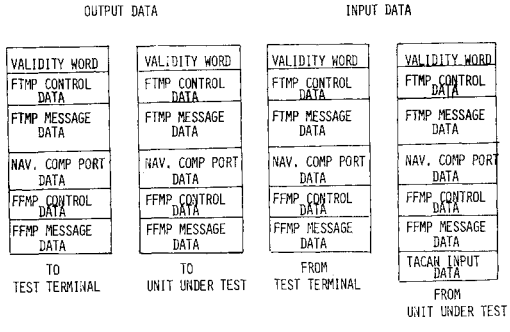

Fig. 4 Terminal port buffers.

Several important features of the test complex are the general purpose computer, the magnetic tape driver, and the keyboard CRT. These three elements are the key elements utilized in testing the JTIDS terminal under all operating conditions. The next section discusses the test methodology of operation.

Test Methodology

A Hewlett Packard 21 MX minicomputer (HP21 MX) is used to control, test, and verify test results. The facility has been built to simplify testing and ease operator/test facility interactions. In order to achieve this, the testing of various operations of the terminal or unit under test were separated into specific test plan sequences; all the test plans were tied to one another by an intermediary test sequence which keeps the terminals functioning. The facility was designed to minimize manual setup time. The minicomputer cues the operator via the CRT display as to the next step prior to execution of the test selected. The CRT keyboard accepts the operator commands for computer activation. As explained in a previous section, all terminal systems are time-synchronized to one another and time is not easily alterable unless all terminals are changed simultaneously. The testing is set up such that timing

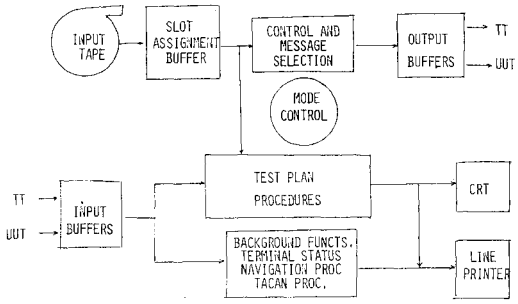

Fig. 5 Program functional overview.

is contiguous between test plans. Most tests provide the operator with test statistics, allowing him to interpret performance. By this means, the terminal's stringent timing coordination is not altered and a test can be repeated, another can be substituted, or the facility can be left in idle while an anomaly is being diagnosed.

A functional overview of the program organization within the HP minicomputer is illustrated in Fig. 5. During a single slot time, the computer must operate with two asynchronous time cycle interrupts issued by the two terminals. As in the real environment, each terminal would issue interrupts to its interfacing processors. After each terminal interrupt, data must be transferred to and from the respective terminal and the minicomputer. Therefore, the original HP minicomputer real-time executive had to be rewritten in order to simulate the parallel processor, as well as to handle the problem and service the faster interrupts. (The HP standard Real Time Executive normally operates in a 50-ms cycle, whereas a 7.8-ms cycle is required for the JTIDS application.) The minicomputer program is designed to handle the test terminal interrupt first, while remembering or waiting to service the interrupt from the UUT terminal. The software is divided into two major segments in order to handle the large amounts of data within the 7.8125-ms time slot. The two segments include the transfer of data to the terminal and the test plan activation, each controlled by the mode (state) control executive.

The first segment, the transfer of data to each terminal, was developed in order to assist and to coordinate each test plan in sending the required messages and control data to each terminal in the correct time slot. Because of the amounts of data to be utilized and handled by the computer, messages and control data are located on magnetic tape in order to alleviate computer storage problems. A record on the tape "drives" the control and message selection process and informs the corresponding test plan when a response is due back from the terminals. The driver tape is segmented into records corresponding to the different parts of the test procedure. A record consists of a record identification, corresponding to a test plan, followed by a large data file broken up into six segments, corresponding to specific message types. These words establish a data bank which is used by the operating test plan. The rest of the record (1½ seconds) consisted of 192 sets of twenty indicators, each indicator corresponding to a location within the data bank. Half the indicators would command the computer to transmit the contents of the respective data bank location to the specified terminal in the then current slot time. The other half would indicate to the current test plan just which data block message in the data bank is expected from which terminal. Tne 20 indicators are each assigned to a slot time. The 192 sets of indicators are utilized because of the cyclic nature assigned to the TDMA slot structure. Each test plan is set up to repeatedly utilize the same 192 slots worth of information until completion of the test. The input tape driver record design is illustrated in Fig. 6. Upon command of each test plan's preliminary setup procedure, the appropriate tape record is read into one of the dual set of slot assignment control buffers. In each time slot,

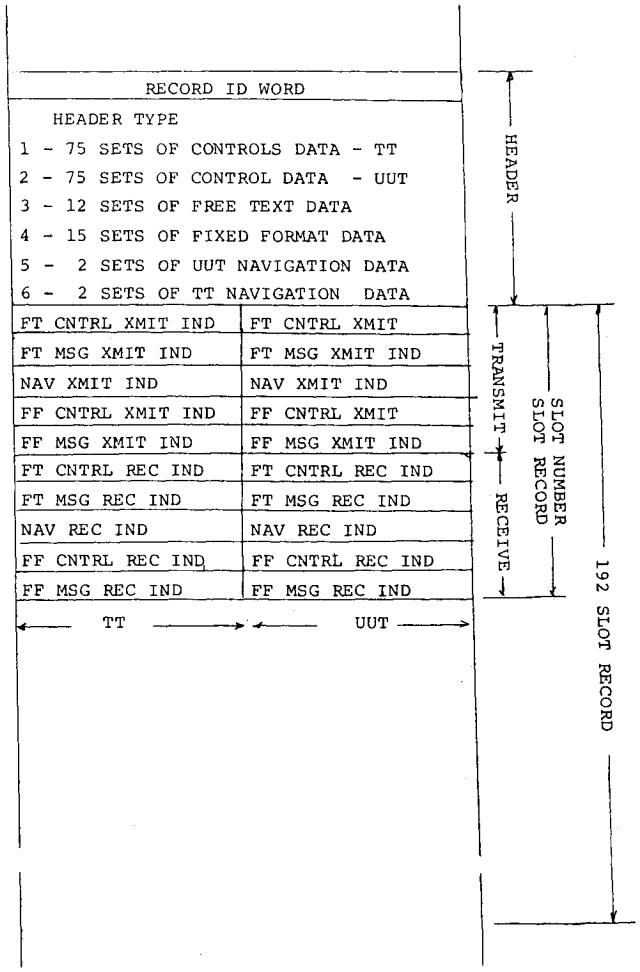

Fig. 6 Driver tape record design.

the control block and message selection process interrogates the corresponding slot transmit indicators for each terminal from the slot buffer. Any positive indication would cause a transfer from the appropriate data bank location, indicated by the indicator, to the appropriate output buffer location (Fig. 4) for transfer to the terminals in the next slot.

The second segment of the minicomputer program includes the test plan procedures and background functions. One of the background functions periodically monitors the status of each terminal and presents these to the operator via the CRT display. Another background function simulates a dead-reckoning system. The test-set supplies to the terminal being tested simulated dead-reckoning navigation data to test the terminal's relative navigation function. The TACAN processing background function is used when the terminal is in the various TACAN operating modes selected by the MCU. It converts the TACAN digital output data from the terminal into proper units for display on the CRT. The TACAN processing performance will be checked by the operator.

The actual testing of the terminals in a simulated real-world environment is segmented into individual test plans. Each test plan is used to check out a particular subset of the terminal's capabilities. Figure 7 illustrates the test-plan-state flow diagram utilized by the minicomputer's mode control to assist the operator in the smooth transition between each test plan. When both terminals are independently powered up and the HP is turned on, the computer enters state 1, which initializes the HP computer. At this time an initialization record is read from the input driver tape. The computer requests a list of inputs from the operator via the CRT. These inputs are required to initialize each terminal for the next test plan. Subsequent test plans will reinitialize the terminals to meet the requirements of that specific test plan.

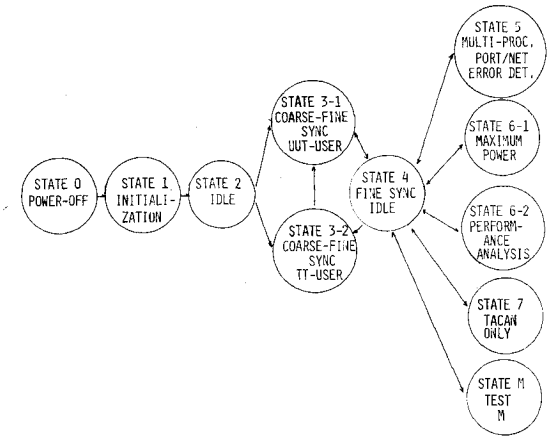

Fig. 7 State flow.

Upon completion of initialization, the mode control switches to initial idle mode (state 2). This state, as well as state 4, the fine sync idle mode, is utilized to smooth the transition between test plans. State 2 will provide required data to each terminal in order to keep them running smoothly while the operator sets up for the next test. The operator is queried via the CRT keyboard as to which coarse-sync/fine-sync test is to be performed. Prior to entering state 3, the operator must set the mode control unit to the desired TDMA operating position.

State 3 is the test plan that tests coarse synchronization and fine synchronization operation. Coarse sync is defined as the ability of the entering terminal to set up its slot structure such that it is synchronized to community time. This is achieved when the terminal looks for a specific time in the time spectrum and receives a message that the community transmits at that time. Fine synchronization is defined as the ability of the entering terminal to fine tune the start of each slot to that of the community. When the system is fine synchronized, the terminal is capable of transmitting messages. The test plan, depending on operator selection, can designate either of the two terminals as the community controller and the other as the user who enters the community. The HP minicomputer supplies messages to both UUT or TT terminals during coarse sync, only expecting to have the user (UUT) receive a message at the specific net entry time. During fine sync, messages are provided to both terminals. The user terminal (UUT), which is trying to achieve fine sync, will receive messages during this time and inhibit all messages for transmission until it has reduced the time-synch error to an acceptable tolerance. The time to coarse synchronize and fine synchronize are recorded. If these are acceptable, control immediately passes to state 4, the fine sync idle mode.

The terminal can be kept in state 4 indefinitely. Messages are provided to each terminal for transmission to one another in order to maintain time synchronization and navigation computation capability. The operator can decide which test plan to proceed to next, namely states 5, 6, or 7.

State 5 is called the multiprocessing test plan. This test plan tests three major functions of the TDMA terminal: the capability of having all terminal ports activated simultaneously; the ability to transmit and receive on different nets; and the ability of the error correction detection circuitry to correct for message errors. The three tests are combined into one test plan for convenience. Each of the three tests are done in sequence within the 192 time slot structure allocated to the test plan. The multiport check tests the capability of the terminal to accept messages at each input port (free test and fixed format) simultaneously for transmission while passing data out of either port, and to receive data on the RF link. These test the terminal at its maximum data rate capability. Various combinations of these coordinated events are per-

formed. The timing and slot structure are prearranged for both terminals as part of the initialization function, state 1, and in the construction of the driver tape for this test. The test passes when the HP minicomputer correctly receives all of the data messages in the required sequence. The capability of terminals to transmit and receive on different nets is also tested. All these net changes are either prearranged by initialization or are specified on demand via the free text port.

The third test in this sequence consists of testing the Reed Solomon message encoder-decoder.[1,2] The Reed Solomon code method used by JTIDS terminals employs a very efficient algebraic (noncryptographic) error-detecting and -correcting algorithm. Most TDMA messages are transmitted after passing through a Reed Solomon message encoder. The message, upon receipt by a terminal, is decoded by the Reed Solomon method for correcting transmission-path-induced errors. The Reed Solomon code is capable of correcting a total of 16 erasures or 8 errors in each 31-symbol data block. To test the decoding operation, corrupted Reed Solomon encoded messages have been devised prior to testing with intentional errors, some of which can be decoded properly, but others of which cannot. These messages are then transmitted from the test terminal by causing that terminal's output circuitry to bypass the encoding process. The received messages are checked for expected receipt condition, as well as compared to the original plain text message. Any errors are printed on the line printer along with the expected and received error statistics. To test the erasure capability, the test terminal is commanded to send a very short message, while the receiving terminal (UUT) is expecting a normal-length message. The receiving terminal therefore should declare erasures since no signal is present. At the end of the requested number of cycles (192 slots) in state 5, the test plan returns to state 4.

State 6 is a service test plan. The test plan first reinitializes each terminal's slot assignments prior to the execution of the next test, which is determined by the driver tape. The first part of the test plan verifies the ability of the terminal to transmit maximum power for a sustained period of time. The unit under test is commanded to transmit messages in sequential slots until the specified limit is reached. The terminal is then made to receive for the remaining period of the prescribed power on/off cycle without losing any messages. During this test, oscilloscopes and an RF power meter will be attached to the RF port. During the second half of the test, the ability of the UUT to measure the time of arrival receipt within the slot is summed and the standard deviation and mean are printed on the line printer after a large sample of received messages has been processed. At the conclusion of this test, each terminal is reinitialized to its original slot assignment prior to returning to state 4.

State 7, the TACAN-only mode, is also a service test mode. In this mode, the unit under test is changed from TDMA processing to TACAN-only processing. A TACAN simulator will be attached to the RF port and transmissions between the terminal and a simulated TACAN beacon will be initiated. The HP minicomputer will convert TACAN data for display on the CRT provided by the terminal. In addition it will display digital TACAN information obtained from the TACAN signal processing function located in the terminal. At the end of the test, return to state 4 is initiated.

These seven test plans are currently all that are used to test the terminal hardware/software interrelations. Many additional tests will probably be devised to further evaluate terminal functions during the course of the program.

Summary

The JTIDS class II terminal which uses a TDMA data link has been developed and is now being evaluated. The minicomputer-based test facility developed to check the terminal performance is considered to be a relatively simple and inexpensive method of testing and evaluating a complex digital information transfer device. The techniques developed represent an optimal distribution of data processing tasks between required real-time processing by the test complex minicomputer and adequate utilization of predetermined message sequences which circumscribe the demands made on the somewhat limited memory of that minicomputer.

Acknowledgment

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